REMARKS

The Office Action dated September 30, 2003, was carefully reviewed. Claim 1 has been amended. Claims 1-13 remain in the application. It is respectfully requested the Examiner reconsider the present application in light of the remarks herein.

The Examiner rejected claims 1-9 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,138,185 to Nelson et al., hereinafter Nelson.

Applicant's amended independent claim 1 requires synchronizing the operation of the I/O shifter using the clock signal and the latch signal. Similarly, independent claim 5 serializes parallel data and requires serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal. These features are not disclosed in Nelson. In the present invention the software is responsible for the control of each serial I/O shifter and each I/O shifter can be enabled or disabled any time through software commands. The operation of all the serial I/O shifters is synchronized to their respective clock and latch signals. The operation of the serial I/O shifters becomes transparent to the software, and once the shifters are enabled, their operation is autonomous.

Nelson discloses a clock signal coupled to each PRC and each port. However, the clock signal does not synchronize I/O shifters as taught by the present invention. Nelson teaches the clock signal is used to indicate an encoding that identifies the actual request type, and more clock signals can be used to provide a greater number of encodings so as to indicate a wider variety of request types. This is significantly different from the present invention.

It is respectfully asserted that the present invention is not anticipated by the Nelson reference. It is respectfully requested the Examiner withdraw the rejection of claims 1-9 under 35 U.S.C. § 102.

The Examiner rejected claims 10-13 under 35 U.S.C. § 103 as being unpatenable over Nelson in view of U.S. Patent No. 6,301,509 to Obata. The Examiner asserted that Nelson discloses all of the limitations of claim 10 except reconstructing the serial data into parallel I/O signals in a serial I/O shifter. The Examiner asserted that it would have been obvious to combine Nelson with Obata to achieve the present invention. It is respectfully asserted that this is not so.

The present invention is directed to the problem of design inflexibility for I/O usage. To overcome this problem the present invention teaches a microprocessor based I/O system that transfers I/O signals between system devices using both serial and parallel signal pathways. To accomplish this objective the present invention teaches an I/O crossover switching network having a plurality of I/O shifters, a clock generator and I/O control logic to provide an I/O multiplexer and pin controller with serial and parallel capabilities.

The present invention allows a designer to independently select I/O signals for serial transfer and I/O signals for parallel transfer using several different serial timing protocols.

The present invention teaches reconstructing serialized data for communication with a parallel device. Parallel reconstruction begins on the assertion of a latch signal to the external device. Thereafter, serial I/O data from the external device is clocked into the serial I/O shifter. Once all "n" bits of the serial

I/O data stream have been clocked into the shifter, the shifter reconstructs the serial data into parallel I/O signals. The parallel I/O signals are then output to the I/O crossover-switching network.

Nelson is directed to the problem of blocked port requests for multi-port connection devices. Subsequent connection requests are blocked until a first connection request is processed. Another drawback addressed by Nelson is the lack of knowledge about whether a destination port is busy before processing the connection request. To overcome this problem Nelson proposes a switch that couples a plurality of port request controllers (PRCs) to its own I/O port. A plurality of serial request busses is arranged such that each serial request bus is coupled to each PRC with its associated I/O port. A plurality of serial response busses is coupled such that each serial response bus is coupled to each PRC with its associated port. Nelson teaches processing multiple requests for connection concurrently, or in a parallel fashion, but does not teach serialization of parallel data or reconstruction of serial data into parallel data as taught by the Applicant of the present invention.

The present invention teaches serialization and de-serialization that is synchronized to the clock cycle. For serialization, the signals are sampled on the first edge of the latch signal and transferred at the rate of one bit per clock cycle. For de-serialization, parallel reconstruction begins on the latch signal. Thereafter, serial I/O data is clocked into the serial I/O shifter from the external device into the serial I/O shifter at the rate of one bit per clock cycle.

Obata discloses a serial communication circuit that converts parallel signals from the CPU to serial signals that are sent to a control unit. But does not teach synchronization of a plurality of I/O shifters as taught by the present invention, nor does Obata teach synchronized reconstruction of a serial I/O data stream into parallel I/O.

One skilled in the art would not look to combine the Nelson and Obata references to achieve applicant's invention. Nelson is directed to the problem of directing signals to avoid blocking signal transmission because of busy ports and proposes processing connection requests in parallel. Obata is directed to a CPU for high speed data communication and discloses a circuit that converts parallel signals to serial signals. The present invention is directed to design inflexibility for transferring I/O signals between system devices that use both serial and parallel signal pathways. The present invention teaches independent selection of I/O signals for serial transfer and I/O signals for parallel transfer.

Further, merely combining Nelson and Obata would not result in the Applicant's invention. Nelson teaches processing connection and clear requests concurrently to avoid blocking signals at busy ports. The clock signal is Nelson is used to encode requests. Obata discloses a serial communication circuit that converts parallel signals output from the CPU into serial signals. The combination of Nelson and Obata would not result in a synchronous transfer of serial data and reconstruction of parallel I/O signals from an incoming serial data stream as taught by the applicant of the present invention.

Should the Examiner have any questions or comments that may place the application in better condition for allowance, he is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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